200G QSFP56 Direct Attach Passive Copper Cable

Features

- Compatible with IEEE 802.3bj and IEEE 802.3cd
- In accordance with the paging function in the protocol SFF-8636, paging can be selected 00H or 02H in 127 bytes
- Supports aggregate data rates of 200Gbps(PAM4)
- Optimized construction to minimize insertion loss and cross talk
- Backward compatible with existing QSFP+ connectors and cages
- Pull-to-release slide latch design
- 26AWG through 30AWG cable
- Straight and break out assembly configurations available
- Customized cable braid termination limits EMI radiation
- Customizable EEPROM mapping for cable signature
- RoHS compliant

Applications

- Switches,servers and routers
- Data Center networks
- Storage area networks
- High performance computing
- Telecommunication and wireless infrastructure
- Medical diagnostics and networking
- Test and measurement equipment

Compliance

- 200G Ethernet (IEEE 802.3cd)
- SFF-8665
- 108-32081 QSFP28 Copper Module Direct Attach Cable Assembly

Description

QSFP56 passive copper cable assembly feature eight differential copper pairs,providing four data transmission channels at s peeds up to 56Gbps(PAM4) per channel,and meets 200G Ethernet requirements.Available in a broad rang of wire gauges-fro m 26AWG through 30AWG-this 200G copper cable assembly features low insertion loss and low cross talk.

QSFP56 uses PAM4 signals for transmission, which doubles the rate. However, there are more stringent requirements for c able insertion loss. For detailed requirements, please see High Speed Characteristics.

Designed for applications in the data center,networking and telecommunications markets that require a high speed,reliable c able assembly,this next generation product shares the same mating interface with QSFP+ form factor ,making it backward c ompatible with existing QSFP ports.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Storage Temperature	TSTG	-40	-	+85	°C	
Operating Case Temperature	Tc	0		+70	°C	
Power Supply Voltage	VCC3	3.14	3.3	3.47	V	
Data Rate Per Lane		1	-	28	Gb/s	

High Speed Characteristics

Table2-High Speed Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Differential Impedance	TDR	90	100	110	Ω	
Insertion loss	SDD21	-16.06			dB	At 13.28 GHz
Differential Return Loss	SDD11 SDD22			See1	dB	At 0.05 to 4.1 GHz
				See 2	dB	At 4.1 to 19 GHz
Common-modeto common-mode output return loss	SCC11 SCC22			-2	dB	At 0.2 to 19 GHz
Differential to common-mode return loss	SCD11			See 3	dB	At 0.01 to 12.89 GHz
	SCD22			See 4		At 0.01 to 12.89 GHz
Differential to common Mode Conversion Loss	SCD21-IL			-10	dB	At 0.01 to 12.89 GHz
				See 5		At 12.89 to 15.7 GHz
				-6.3		At 15.7 to 19 GHz

Notes:

Reflection Coefficient given by equation SDD11(dB) ≤ -16.5 + 2 × SQRT(f), with f in GHz

Reflection Coefficient given by equation SDD11(dB) ≤ -10.66 + 14 × log10(f/5.5), with f in GHz

Reflection Coefficient given by equation SCD11(dB) ≤ -22 + (20/25.78)*f, with f in GHz

Reflection Coefficient given by equation SCD11(dB) ≤ -15 + (6/25.78)*f, with f in GHz

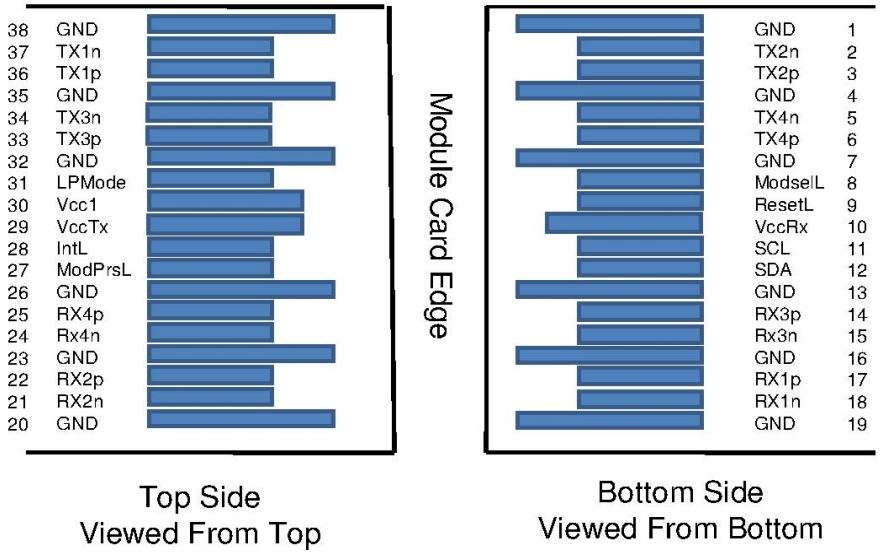
Reflection Coefficient given by equation SCD21(dB) ≤ -27 + (29/22)*f, with f in GHz

Pin Descriptions

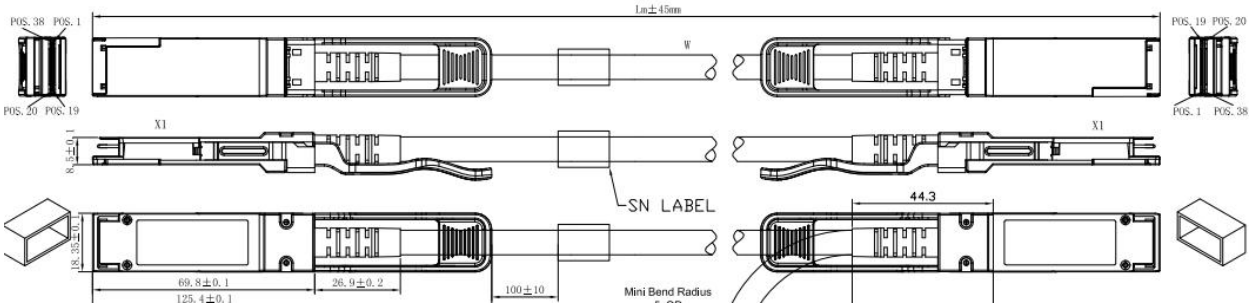
Table3- Pin Function Definition

Pin	Logic	Symbol	Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ModSelL	Module Select	
10		Vcc Rx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Outpu	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1p	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output Ground	

26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		Vcc Tx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1



Mechanical Specifications



Length (m)	Cable AWG
1	30
2	26/30
3	26

Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.7	Class 1(→2000 Volts)
Electromagnetic Interference(EMI)	FCC Class B	Compliant with Standards
	CENELEC EN55022 Class B	
	CISPR22 ITE Class B	
RF Immunity(RFI)	IEC61000-4-3	Typically Show no Measurable Effect from a 10V/m Field Swept from 80 to 1000MHz
RoHS Compliance	RoHS Directive 2011/65/EU and it's Amendment Directives 6/6	RoHS 6/6 compliant