400G QSFP-DD to 2x200G QSFP56 Active Optical Breakout Cable

Features

- 400Gb/s to 2x200Gb/s data rate
- 8x 50Gb/s PAM4 modulation
- Single 3.3V power supply
- Max 4.5W power dissipation each QSFP56 end
- Max 8W power dissipation QSFP-DD end
- Compliant to CMIS V4.0
- Operating case temp Commercial: 0°C to +70 °C
- Hot pluggable
- RoHS compliant

Applications

- 400Gb/s systems
- Other optical links

Standards

- IEEE 802.3cd
- QSFP-DD MSA
- QSFP-DD-CMIS-Rev 4.0
- IEEE 802.3bs Annex120E
- SFF-8024 Rev. 4.6
- SFF-8679 Rev1.8
- SFF-8665 Rev1.9

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Storage Temperature Range	TS	-5	-	+75	℃	
Relative Humidity	RH	+5	-	+85	%	
Power Supply Voltage	VCC	-0.5	-	+3.6	V	

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbol	Unit.	Min	Typ.	Max	Note
Operating Case Temperature Range	Tc	℃	0		70	
Power Supply Voltage	VCC	V	3. 14	3.3	3.47	
Power dissipation (400G retiming on all lanes)	Pd400G	W	-	-	8	
Power dissipation (200G retiming on all lanes)	Pd200G	W	-	-	4.5	

Electrical Characteristics

Table3-Electrical Characteristics

Parameter	Symbol	Unit	Min.	Typical	Max.	Note
Transmitter						
Signaling rate (each lane)	SR	GBd	26.5625 ± 100 ppm			
Differential data input voltage per lane	Vin,pp,diff	mV	-	-	900	
Differential termination mismatchal	-	%	-	-	10	
Single-ended voltage tolerance range	-	V	-0.4	-	3.3	
DC common mode voltage	-	mV	-350	-	2850	
Receiver						
Signaling rate (each lane)	SR	GBd	26.5625 ± 100 ppm			
Differential output voltage	-	mV	-	-	900	
Differential termination mismatch	-	%	-	-	10	
Transition time (min, 20% to 80%)	-	ps	9.5	-	-	

DC common mode voltage	-	mV	-350	-	2850	
Error Bit Rate	BER	-	-	-	2.4E-4	1

Notes:

1. PRBS31Q@26.5625Gbd PAM4

Recommended Interface Circuit

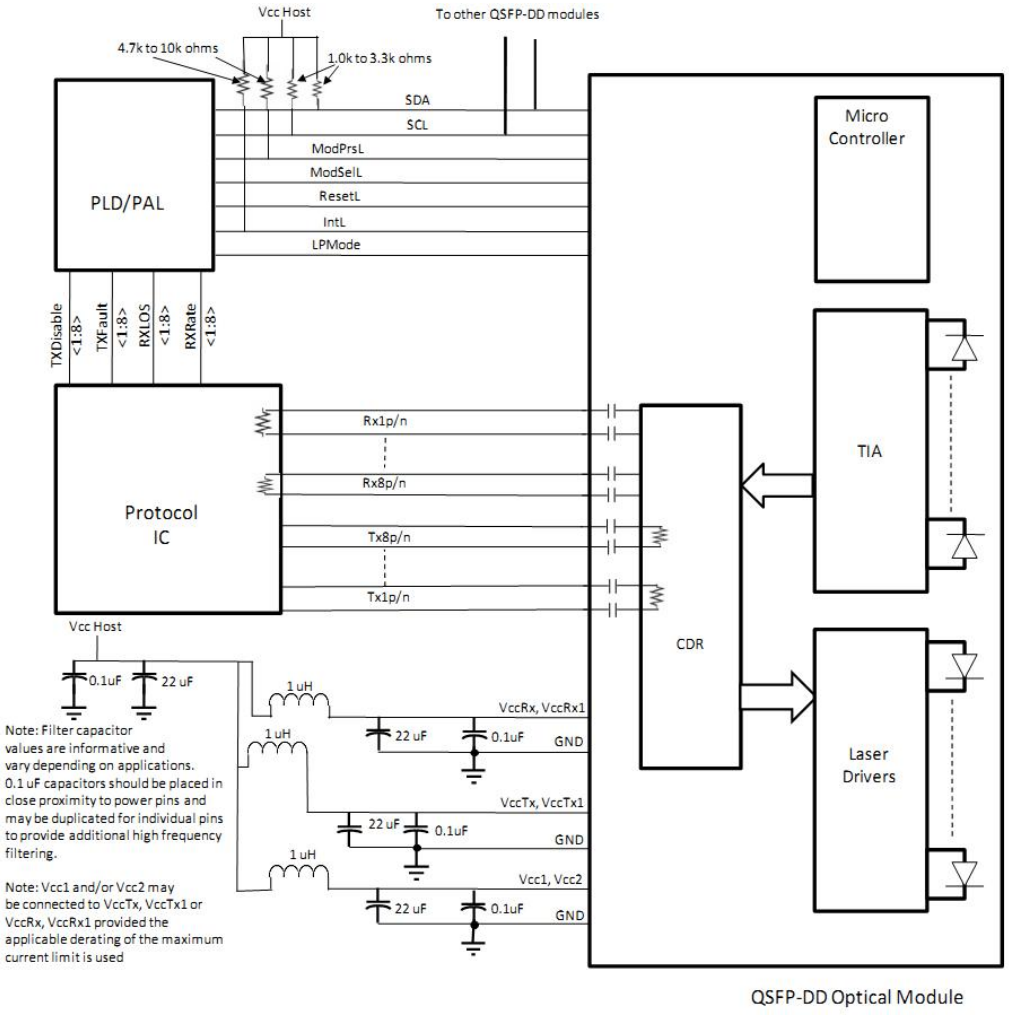

Figure 1 Recommended Interface Circuit

Pin Descriptions

1. 400G QSFP-DD

Table4- Pin Function Definition

Pin	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16	GND	GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	1
18	CML-O	Rx1n	Receiver Inverted Data Output	1
19		GND	Ground	
20		GND	Ground	
21	CML-O	Rx2n	Receiver Inverted Data Output	1
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	
27	LVTTL-O	ModPrsL	Module Present	2
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636)	2
29		VccTx	+3.3V Power supply transmitter	
30		Vcc1	+3.3V Power supply	1
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	
32		GND	Ground	
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	1

34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	1
37	CML-I	Tx1n	Transmitter Inverted Data Input	1
38		GND	Ground	
39		GND	Ground	
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		VccRx1	3.3V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future Use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69		Reserved	For future Use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	

76		GND	Ground	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). A ll the common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connected theses directly to the host board signal common ground plane.

2. VCCRx, VCCRx 1, VCC1, VCC2, VCCTx, and VCCTx 1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4 . VCCRx, VCCRx 1, VCC 1, VCC2, VCCTx, and VCCTx 1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor Specific and Reserved pads shall have an impedance to GND that is greater than 10kOhms and less than 100pF.

QSFP-DD end

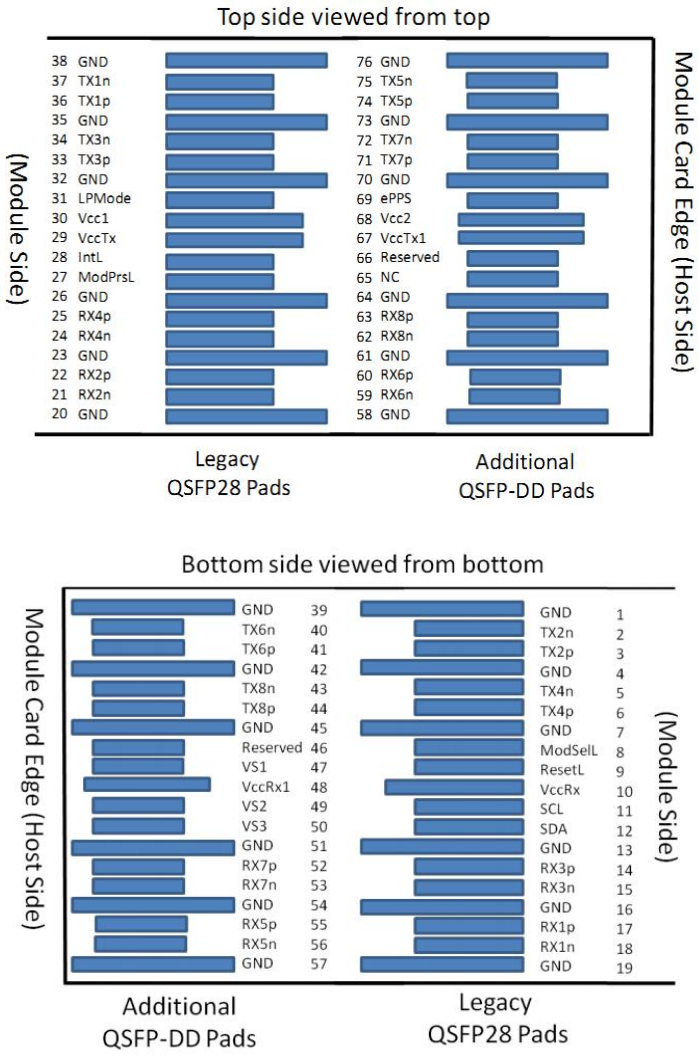

Figure 2. Pin View for QSFP-DD

2.100G QSFP56

Table5- Pin Function Definition

Pin	Symbols	Logic	Description	Notes
1	GND		Ground	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	
4	GND		Ground	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	
7	GND		Ground	
8	ModSelL	LVTTL-I	Module Select	
9	ResetL	LVTTL-I	Module Reset	
10	Vcc Rx		+3.3V Power Supply Receiver	2
11	SCL	LVCOMS-I/O	2-wire serial interface clock	
12	SDA	LVCOMS-I/O	2-wire serial interface data	
13	GND		Ground	
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	
15	Rx3n	CML-O	Receiver Inverted Data Output	
16	GND		Ground	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	
18	Rx1n	CML-O	Receiver Inverted Data Output	1
19	GND		Ground	1
20	GND		Ground	
21	Rx2n	CML-O	Receiver Inverted Data Output	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	
23	GND		Ground	
24	Rx4n	CML-O	Receiver Inverted Data Output	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	
26	GND		Ground	1
27	ModPrsL	LVTTL-O	Module Present	
28	IntL	LVTTL-O	Interrupt	
29	VccTx		+3.3V Power supply transmitter	2
30	Vcc1		+3.3V Power supply	2
31	LPMode	LVTTL-I	Low Power Mode	
32	GND		Ground	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	
34	Tx3n	CML-I	Transmitter Inverted Data Input	
35	GND		Ground	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	
37	Tx1n	CML-I	Transmitter Inverted Data Input	
38	GND		Ground	1

Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane. 2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 2 below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000mA.

QSFP56 end

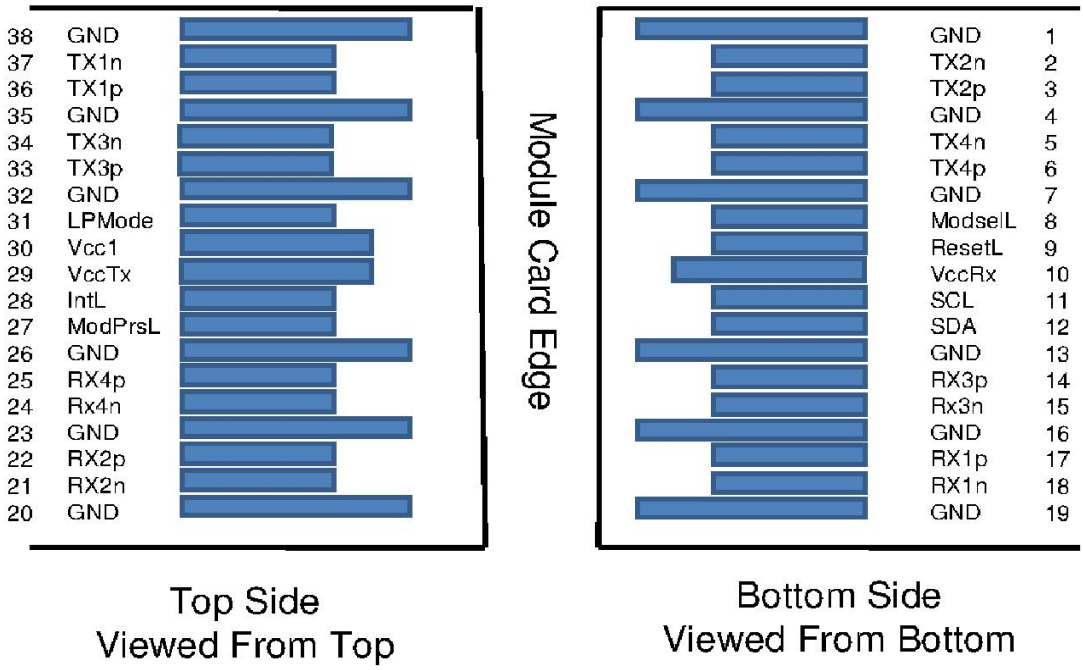

Figure 3. Pin View for QSFP56

Mechanical

1.QSFP-DD endUnit mm

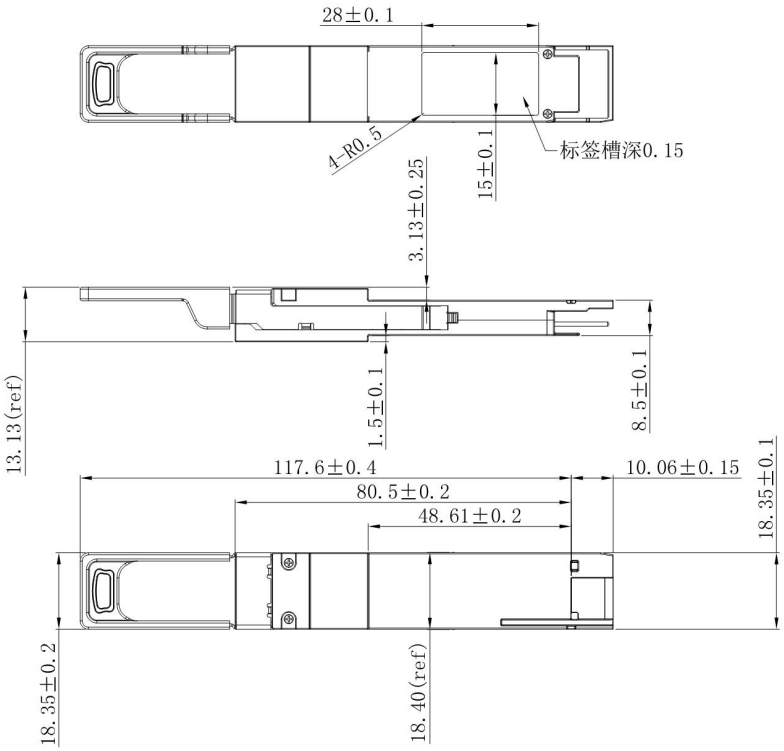

Figure 4. Mechanical Diagram for QSFP-DD

2. QSFP56 end

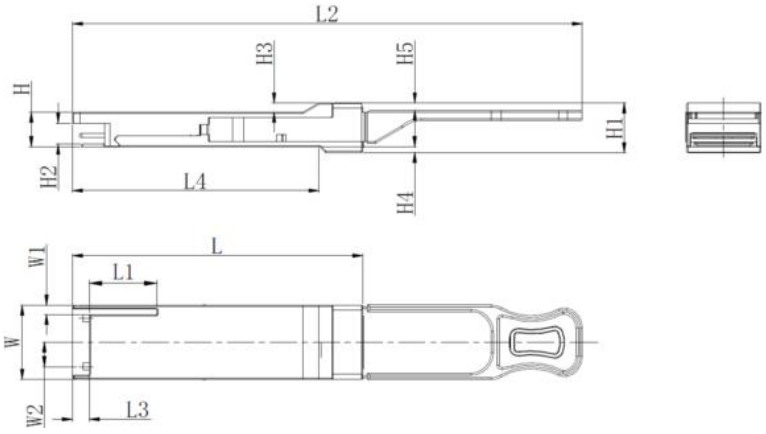

Figure 5. Mechanical Diagram for QSFP56

	L	L1	L2	L3	L4	W	W1	W2	H	H1	H2	H3	H4	H5	H6
Max	72.2	-	128	4.35	61.4	18.45	-	6.2	8.6	12.4	5.35	2.5	1.6	2.0	-
Type	72.0	-	-	4.20	61.2	18.35	-	-	8.5	12.2	5.2	2.3	1.5	1.8	6.55
Min	68.8	16.5	124	4.05	61.0	18.25	2.2	5.8	8.4	12.0	5.05	2.1	1.3	1.6	-

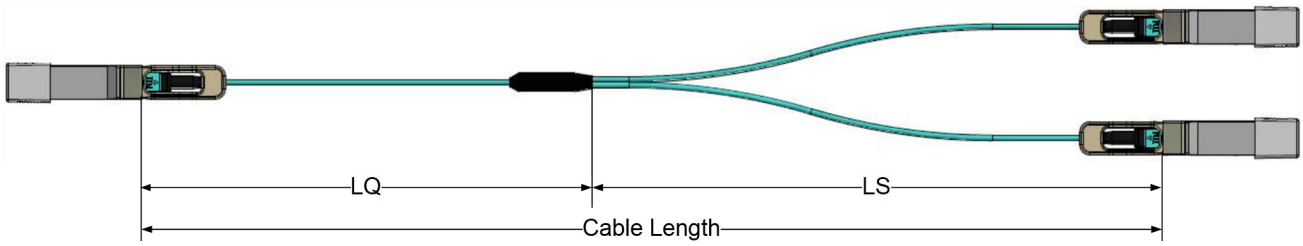

Figure 6. Mechanical Diagram of Cable

Cable Length

Table6-Cable Length

Parameter	Value	Units
Diameter	3±0.2	mm
Minimum bend radius	30	mm
Power Supply Voltage	1 m ≤length ≤ 4.5 m: +15 / -0	cm
	5 m ≤length ≤ 14.5 m: +30 / -0	cm
	Length≥15.0 m +2% / -0	m
Cable color	Aqua	

Breakout Cable Nominal Length

Table7-Breakout Cable Nominal Length

Total Length X (Unit: m)	Breakout Point Measured from QSFP-DD LQ(Unit: m)	Breakout Point Measured from QSFP56 LS(Unit: m)
1	0.3	0.7
2	0.6	1.4
3	1	2
5	2	3
7	4	3
10	7	3
15	12	3
20	17	3
25	22	3
30	27	3
40	37	3
50	47	3

Connectivity Schematic

400Gb/s Side	200Gb/s Side
	Port 1
TX1	RX1
RX1	TX1
TX2	RX2
RX2	TX2
TX3	RX3
RX3	TX3
TX4	RX4
RX4	TX4
	Port 2
TX5	RX1
RX5	TX1
TX6	RX2
RX6	TX2
TX7	RX3
RX7	TX3
TX8	RX4
RX8	TX4