400G Single-port OSFP Single Mode DR4 100m Transceiver

Features

- OSFP MSA 5.0 compliant
- 4x106.25Gb/s PAM4 electrical interface
- Maximum power consumption 9W@ Tcase = 70℃
- 1xMPO-12 APC connector
- Up to 100m transmission on single mode fiber
- Operating case temperature: 0℃~70℃
- RoHS-6 compliant
- Compliant with OSFP MSA Rev5.0, CMIS Rev5.2, IEEE 802.3ck, IEEE 802.3bs and GR-468-CORE

Applications

- Used in ConnectX-7/OSFP adapters linked to Twin-port transceivers in 2x400G switches

Description

The OSFP-400G-DR4 Transceiver is a high performance, cost effective module for optical data communication applications supporting 400G Ethernet. The OSFP-400G-DR4 is designed to operate in switch and router applications supporting OSFP MSA compliant traffic for up to 100m links.

The OSFP-400G-DR4 can convert 4-channel 106.25Gb/s electrical data to 4-channel 106.25Gb/s optical signals. Similarly, it optically converts 4-channel 106.25Gb/s optical signals to 4-channel electrical data output on the receiver side. It has been designed to withstand the maximum range of external operating conditions including temperature, humidity and EMI. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

The Single-port and Twin-port transceiver combinations guarantee optimal operation. Rigorous production testing ensures the best out-of-the-box installation experience, performance, and durability.

Absolute Maximum Specifications

Absolute maximum ratings are those beyond which damage to the device may occur.

Prolonged operation between the operational specifications and absolute maximum ratings is not intended and may cause permanent device degradation.

Table1-Absolute Maximum Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Storage Temperature	TSTG	-40		85	°C
Operating Relative Humidity	RH	5		85	%
Supply Voltage	VCC	-0.5	3.3	3.6	V
Receiver Damage Threshold, each lane		5			dBm

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max.	Units
Case temperature	Tcase	0		70	℃
Supply Voltage	VCC	3.135	3.3	3.465	V
Supply Current	ICC			2871	mA
Module Power Dissipation	P			9	W

Optical, Electrical Characteristic

Tested under recommended operating conditions, unless otherwise noted

Table3-Transmitter Operating Characteristic-Optical, Electrical

Parameter	Symbol	Min	Typical	Max	Units	Notes
Optical Data Rate, each Lane			53.125±100ppm		GBd	
Modulation Format			PAM4			
Line wavelengths	λ	1304.5	1311	1317.5	nm	
Average Launch Power, each lane	PAVG	-2.9		4	dBm	
Optical Modulation Amplitude (OMA), each lane	OMA	-0.8		4.2	dBm	
Extinction Ratio	ER	3.5			dB	
Side-Mode Suppression Ratio	SMSR	30			dB	
Launch power in OMA minus TDECQ, each lane		-2.2			dBm	
Transmitter and Dispersion Eye Closure for PAM4, each Lane	TDECQ			3.4	dB	
Optical Return Loss Tolerance				21.4	dB	
Transmitter Reflectance				-26	dB	
Average Launch Power of OFF Transmitter, each Lane				-15	dBm	
Electrical Data Rate, each lane			53.125±100ppm		GBd	
Differential pk-pk input Voltage tolerance	Vpp	800			mV	
DC Common Mode Voltage	Vcm	-350		2850	mV	Note1
Differential Termination Resistance Mismatch	Rdm			10	%	
Effective return loss				8.5	dB	
Differential to Common Mode Input Return Loss			IEEE 802.3-ck Equation (120G-2)		dB	
Module Stressed Input Test			IEEE 802.3ck 120G.3.4.2			Note2

Notes:

[1] DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

[2] BER specified in IEEE 802.3ck 120G.1.1

Table4-Receiver Operating Characteristic-Optical, Electrical

Parameter	Symbol	Min	Typical	Max	Units	Notes
Optical Data Rate, each Lane			53.125±100ppm		GBd	
Modulation Format			PAM4			
Line wavelengths	λ	1304.5	1311	1317.5	nm	
Average receiver power, each lane		-5.9		4	dBm	

Receiver power, each lane (OMA)				4.2	dBm	
Receiver Sensitivity (OMAouter) , each lane				max(-3.9, SECQ-5.3)	dBm	Note 1
Stressed receiver sensitivity (OMAouter), each laned (max)				-1.9	dBm	
Receiver reflectance				-26	dB	
Electrical Data Rate, each lane			53.125±100ppm		GBd	
Differential Termination Resistance Mismatch		-10		10	%	
Differential output Voltage pk-pk	Vpp			845	mV	
DC Common Mode Voltage	Vcm	-350		2850	mV	Note 2
Effective return loss	ERL	8.5			dB	
Transition time		8.5			ps	
Common mode to differential return loss		IEEE 802.3-CK Equation (120G-1)			dB	

Notes:

[1] Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.

Receiver sensitivity(OMAouter),each lane:

for TDECQ＜1.4dB,max=-3.9(dBm).For 1.4dB＜TDECQ＜3.4dB,max=SECQ-5.3(dBm).

[2] DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Optical Specifications

Table5-Digital Diagnostic Functions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3		3	℃	Note1
Supply voltage monitor absolute error	DMI_Vcc	-3%		3%	V	Note2
Bias current monitor absolute error	DMI_Ibias	-10%		10%	mA	
Laser power monitor absolute error	DMI_Tx	-3		3	dB	
RX power monitor absolute error	DMI_Rx	-3		3	dB	

Notes:

[1] Temperature here is depending on module case around Max power dissipation. Temperature monitor is done over operating temperature.

[2] Supply voltage monitor is done over operating voltage.

Table6-Control and Status I/O Timing Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
MgmtInitDuration	Max MgmtInit Duration			2000	ms	Note1
ResetL Assert Time	t_reset_init	10			μs	Note2
IntL Assert Time	ton_IntL			200	ms	Note3
IntL Deassert Time	toff_IntL			500	μs	Note4

Rx LOS Assert Time	ton_los			100	ms	Note5
Flag Assert Time	ton_flag			200	ms	Note6
Mask Assert Time	ton_mask			100	ms	Note7
Mask Deassert Time	toff_mask			100	ms	Note8

Notes:

[1] Time from power on, hot plug or rising edge of reset until completion of the MgmtInit State.

[2] Minimum pulse time on the ResetL signal to initiate a module reset.

[3] Time from occurrence of condition triggering IntL until Vout:IntL=Vol.

[4] Time from clear on read operation of associated flag until Vout:IntL=Voh.This includes deassert times for Rx LOS, Tx Fault and other flag bits.

[5] Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.

[6] Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.

[7] Time from mask bit set (value=1b) until associated IntL assertion is inhibited.

[8] Time from mask bit cleared (value=0b) until associated IntL operation resumes.

Table7-Surge Current Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
Module power supply voltage including ripple,droop and noise below 100 kHz	Vcc_Modu le	3.135	3.3	3.465	V	
Host power supply voltage including ripple, droop and noise below 100 kHz	Vcc_Host	3.135	3.3	3.465	V	
Module power supply noise tolerance 10 Hz - 10 MHz (peak-to-peak) Voltage drop across mated connector(Vcc_Host minus Vcc_Module)	Vcc_drop			66	mV	
Total current for Vcc pins	Icc_modul e			10	A	Note1
Host RMS noise output 10 Hz-10 MHz	e N_Host			25	mV	
Module RMS noise output 10 Hz - 10 MHz	e N_Mod			15	mV	
Module inrush - instantaneous peak duration	T_ip			50	μs	
Module inrush - initialization time	T_init			500	ms	
Inrush and Discharge Current	I_didt			100	mA/μs	Note2
High power mode to Low power mode transition time from assertion of M_LPWn or M_RSTn or Force Low Pwr	T_hplp			200	μs	
Power Consumption	P_7			9	W	

Notes:

[1] Utilization of the maximum OSFP power rating requires thermal design and validation at the system level to ensure the maximum connector temperature is not exceeded. A recommended design practice is to heatsink the host board power pin pads with multiple vias to a thick copper power plane for conductive cooling.

[2] The specified Inrush and Discharge Current (I_didt) limit shall not be exceeded for all power transient events. This includes hot-plug, hot-unplug, power-up, power-down, initialization, low-power to high power and high-power to low-power.

Pin Description

The device is OSFP MSA Specification for OSFP Octal Small Form Factor Pluggable Module Rev. 1.12 compliant, see www.osfpmsa.org.

Table8-Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	31	GND	Ground
2	Tx2p	Transmitter Non-Inverted Data Input	32	Rx2p	Receiver Non-Inverted Data Output
3	Tx2n	Transmitter Inverted Data Input	33	Rx2n	Receiver Inverted Data Output
4	GND	Ground	34	GND	Grounds
5	Tx4p	Transmitter Non-Inverted Data Input	35	Rx4p	Receiver Non-Inverted Data Output
6	Tx4n	Transmitter Inverted Data Input	36	Rx4n	Receiver Inverted Data Output
7	GND	Ground	37	GND	Ground
8	Tx6p	Transmitter Non-Inverted Data Input	38	Rx6p	Receiver Non-Inverted Data Output
9	Tx6n	Transmitter Inverted Data Input	39	Rx6n	Receiver Inverted Data Output
10	GND	Ground	40	GND	Ground
11	Tx8p	Transmitter Non- Inverted Data input	41	Rx8p	Receiver Non-Inverted Data Output
12	Tx8n	Transmitter Inverted Data Input	42	Rx8n	Receiver Inverted Data Output
13	GND	Ground	43	GND	Ground
14	SCL	2-wire serial interface clock	44	INT / RSTn	Module Interrupt / Module Reset
15	VCC	+3.3V Power	45	VCC	+3.3V Power
16	VCC	+3.3V Power	46	VCC	+3.3V Power
17	LPWn / PRSn	Low-Power Mode / Module Present	47	SDA	2-wire Serial interface data
18	GND	Ground	48	GND	Ground
19	Rx7n	Receiver Inverted Data Output	49	Tx7n	Transmitter Inverted Data Input
20	Rx7p	Receiver Non-Inverted Data Output	50	Tx7p	Transmitter Non-Inverted Data Input
21	GND	Ground	51	GND	Ground
22	Rx5n	Receiver Inverted Data Output	52	Tx5n	Transmitter Inverted Data Input
23	Rx5p	Receiver Non-Inverted Data Output	53	Tx5p	Transmitter Non-Inverted Data Input
24	GND	Ground	54	GND	Ground
25	Rx3n	Receiver Inverted Data Output	55	Tx3n	Transmitter Inverted Data Input
26	Rx3p	Receiver Non-Inverted Data Output	56	Tx3p	Transmitter Non-Inverted Data Input

27	GND	Ground	57	GND	Ground
28	Rx1n	Receiver Inverted Data Output	58	Tx1n	Transmitter Inverted Data Input
29	Rx1p	Receiver Non-Inverted Data Output	59	Tx1p	Transmitter Non-Inverted Data Input
30	GND	Ground	60	GND	Ground

OSFP Module Pad Layout

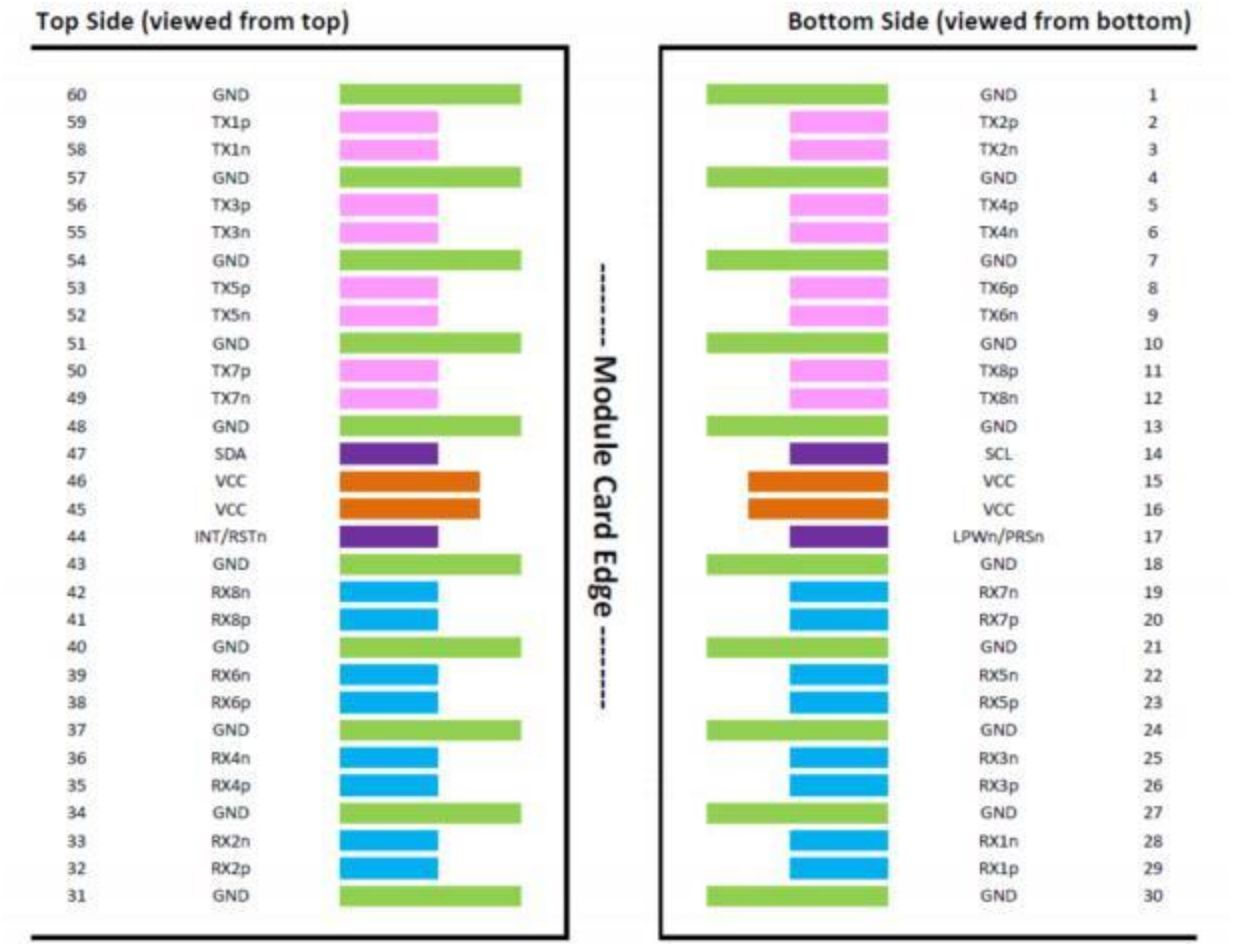

Figure 1 MSA Compliant Connector

Transceiver Block Diagram

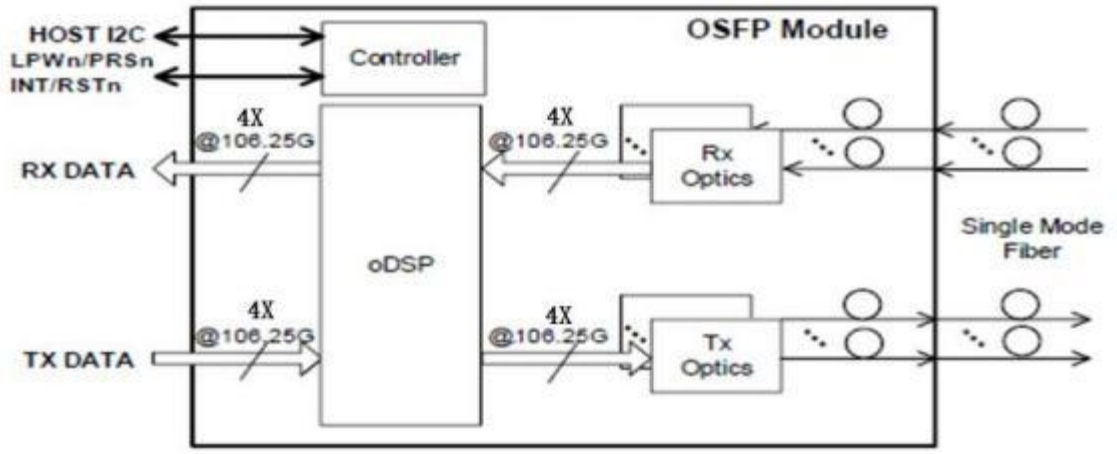

Figure 2 Transceiver Block Diagram

<Transmitter Section>: The transceiver converts 4-channel 106.25Gb/s electrical data to 4-channel 1311nm 106.25Gb/s optical signals for 400Gb/s optical transmission.

<Receiver Section>: Similarly, it optically converts 4-channel 1311nm 106.25Gb/s optical signals to 4-channel electrical data output on the receiver side.

Dimensions

Unit: mm

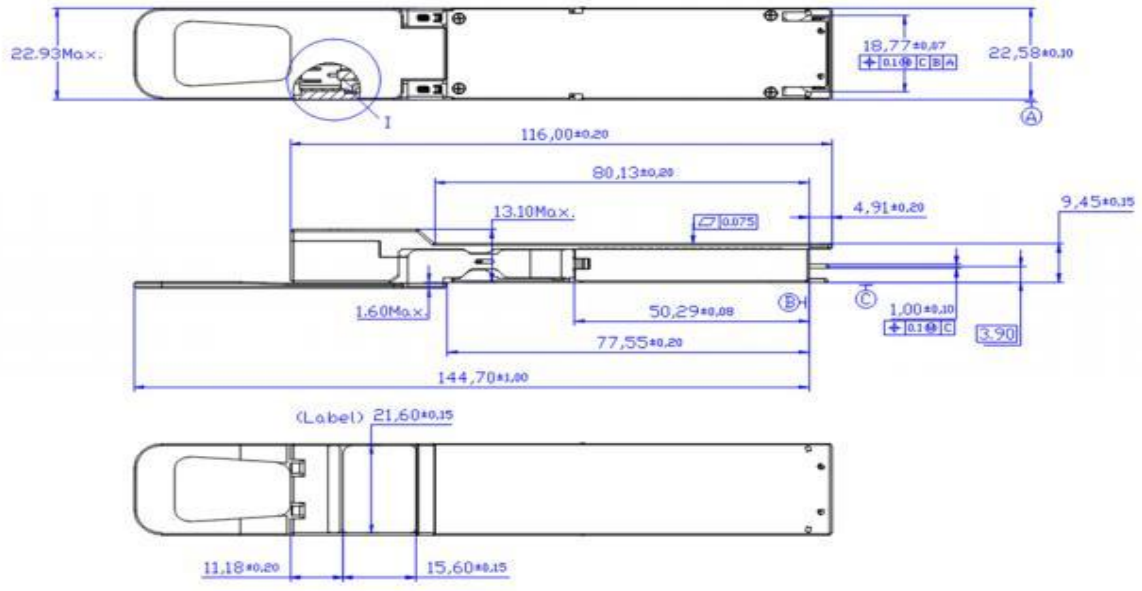

Figure 3 Dimensions of Transceiver

Enlarged view of detail A

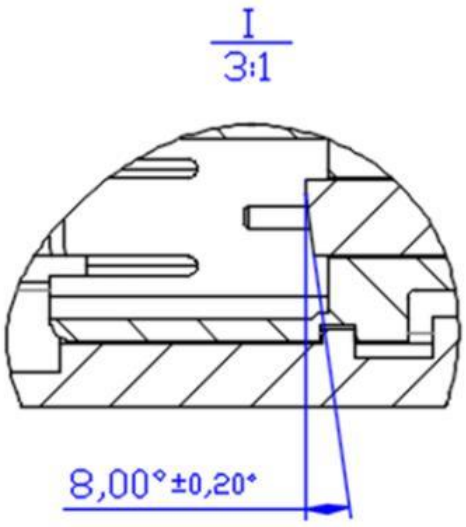

Figure 4 Enlarged view of detail A

Enlarged view of detail B:

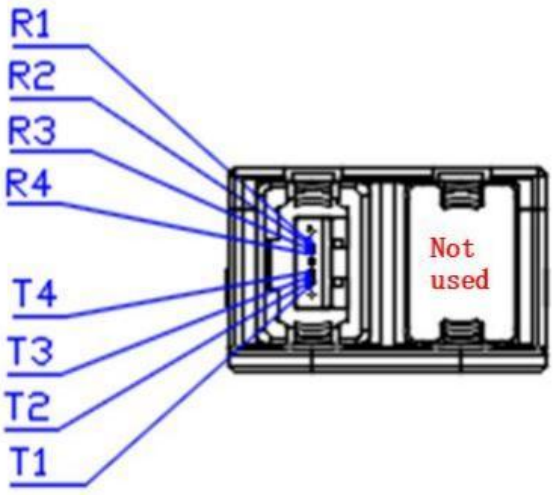

Figure 5 Enlarged view of detail B

Digital Diagnostic Memory Map

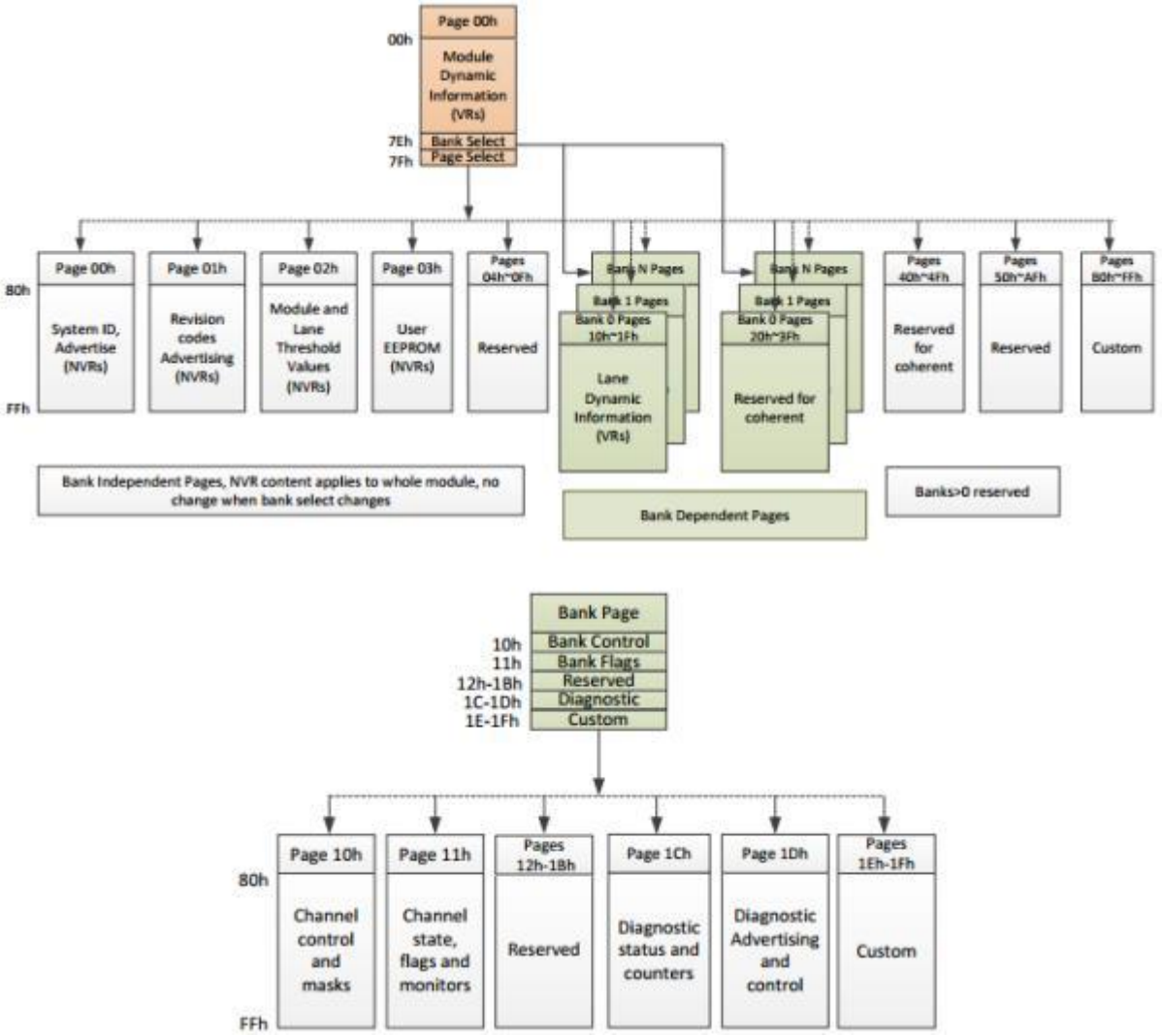

Figure 6 Digital Diagnostic Memory Map

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