400Gb/s QSFP-DD SR4 MPO-12 100m Optical Transceiver

Features

- QSFP-DD MSA compliant
- CMIS compliance
- Optical Interface: IEEE 802.3db compliant
- Electrical Interface: IEEE 802.3 2022 400GAUI-8
- Support 425Gb/s aggregate bit rate
- 4 Parallel optical lanes
- MPO-12 optical connector
- Maximum link length of 70m on OM3 or 100m on OM4
- Operating case temperature 0 to 70℃
- Maximum power consumption 8W

Applications

- Data Center Interconnect
- 400G Ethernet

General Description

The QDD-400G-SR4 transceiver is a 400Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) optical module designed for 100m optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of optical signals, and multiplexes them into a single channel for 400Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 400Gb/s optical input into 4 channels of optical signals, and converts them to 8 channels of 50Gb/s (PAM4) electrical output data.

An optical fiber cable with an MPO-12 connector can be plugged into the QSFP-DD SR4 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through a QSFP-DD MSA-compliant edge type connector.

This product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD MSA Type2. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

I2C interface is supported to read and control the status of this product.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbols	Min.	Max.	Unit	Notes
Storage Temperature	T_S	-40	85	℃	
Operating Case Temperature	T_{OP}	0	70	℃	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_{op}	0		+70	℃	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			53.465		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Link Distance with OM4	D	2		100	m	1
Link Distance with OM3	D	2		70	m	1

Notes:

[1] FEC required on host system to support maximum transmission distance.

Electrical Characteristic

Table3-Electrical Characteristic

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Supply current	Icc			2.55	A	
Power Consumption				8	W	
Module input (each Lane)						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	
Differential pk-pk Input Voltage Tolerance	TP1a	900			mV	
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2022 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2022 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3 2022 120E.3.4.1				
Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3			V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	
Module output (each Lane)						
Signaling Rate, each lane	TP4	26.5625 ± 100 ppm			GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mV	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2022 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2022 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	

Far-end Eye Height,Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
DC Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

Optical Characteristics

Table4-Optical Characteristics

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Transmitter						
Data Rate, each Lane			53.125 ± 100 ppm		GBd	
Modulation Format			PAM4			
Center Wavelength	λ	844	850	863	nm	
RMS Spectral Width	Δ λ rms			0.6	nm	1
Average Launch Power, each Lane	P_{AVG}	-4.6		4	dBm	
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	P_{OMA}	-2.6(For max (TECQ,TDECQ) ＜1.8 dB) -4.4 + max(TECQ,TDECQ) （For 1.8＜ max (TECQ, TDECQ)≤ 4.4 dB)		3.5	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			4.4	dB	
Transmitter eye closure for PAM4, each Lane	TECQ			4.4	dB	
Overshoot/undershoot				29	%	
Transmitter power excursion, each Lane				2.3	dBm	
Extinction Ratio	ER	2.5			dB	
Transition Time	T_t			17	ps	
Optical Return Loss Tolerance	TOL	14			dB	

Average Launch Power of OFF Transmitter, each Lane	Poff			-30	dBm	
$RIN_{14}OMA$	RIN			-132	dB/Hz	
Encircled Flux		⩾ 86% at 19 μm ⩽ 30% at 4.5 μm				2
Receiver						
Data Rate, each Lane		53.125 ± 100 ppm			Gbps	
Modulation Format		PAM4				
Center Wavelength	λ	842		948	nm	
Damage Threshold, each Lane	TH_d	5			dBm	3
Average Receive Power, each Lane		-6.4		4	dBm	4
Receive Power (OMA_{outer}), each Lane				3.5	dBm	
Receiver Sensitivity (OMA_{outer}), each Lane	SEN			-4.6(For TECQ ⩽1.8 dB) –6.4 +TECQ（For 1.8＜TECQ⩽4.4 dB)	dBm	5
Receiver Reflectance	R_R			-15	dB	
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-2.0	dBm	6
LOS Assert	LOSA	-15			dBm	
LOS De-assert	LOSD			-9.4	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Conditions of Stress Receiver Sensitivity Test (Note 7)						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test				4.4	dB	
OMAouter of each aggressor lane				3.5	dBm	

Notes:

[1] RMS spectral width is the standard deviation of the spectrum.

[2] If measured into type A1a.2 or type A1a.3, or A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4.

[3] The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

[4] Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

[5] Receiver sensitivity (OMAouter) is informative and is defined for a transmitter with a value of TECQ up to 4.4 dB. Receiver sensitivity should meet Equation (1), which is illustrated in Figure 1.

RS= max(−4.6, TECQ − 6.4) dBm (1)

Where:

RS is the receiver sensitivity, and

TECQ is the TECQ of the transmitter used to measure the receiver sensitivity.

[6] Measured with conformance test signal at TP3 for the BER equal to $2.4x10^{-4}$.

[7] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

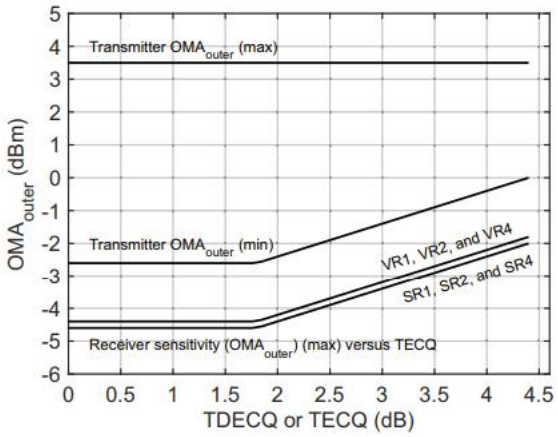

Figure 1 Illustration of Receiver Sensitivity Mask for 400G-SR4

Pin Function Definitions

Table6-Pin Function Definitions

Pin	Logic	Symbol	Description	Notes
1		GND	Ground	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
4		GND	Ground	1B
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B
7		GND	Ground	1B
8	LVTTL-I	ModSelL	Module Select	3B
9	LVTTL-I	ResetL	Module Reset	3B
10		Vcc Rx	+3.3V Power Supply Receiver	2B
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B
13		GND	Ground	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16	GND	GND	Ground	1B
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B
19		GND	Ground	1B
20		GND	Ground	1B

21	CML-O	Rx2n	Receiver Inverted Data Output	3B
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground	1B
24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground	1B
27	LVTTL-O	ModPrsL	Module Present	3B
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636)	3B
29		VccTx	+3.3V Power supply transmitter	2B
30		Vcc1	+3.3V Power supply	2B
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B
32		GND	Ground	1B
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
35		GND	Ground	1B
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B
39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
42		GND	Ground	1A
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A
45		GND	Ground	1A
46		Reserved	For future use	3A
47		VS1	Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49		VS2	Module Vendor Specific 2	3A
50		VS3	Module Vendor Specific 3	3A
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A

61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
64		GND	Ground	1A
65		NC	No Connect	3A
66		Reserved	For future Use	3A
67		VccTx1	3.3V Power Supply	2A
68		Vcc2	3.3V Power Supply	2A
69		Reserved	For future Use	3A
70		GND	Ground	1A
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A
73		GND	Ground	1A
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A

Pin Map and Description

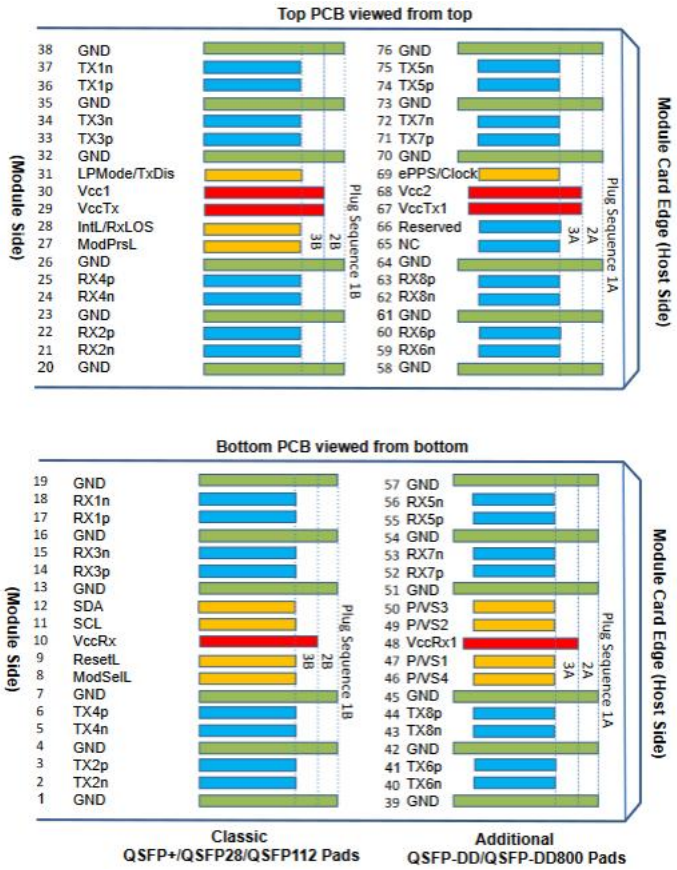

Figure 2 Pin Map and Description

QSFP-DD Control pins

Name	Direction	Description
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host
SDA	BiDir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host
IntL/RxLOS	Output	Active low IntL output port only
LPMode/TxDis	Input	Active high LPMode input port only

Transceiver Block Diagram

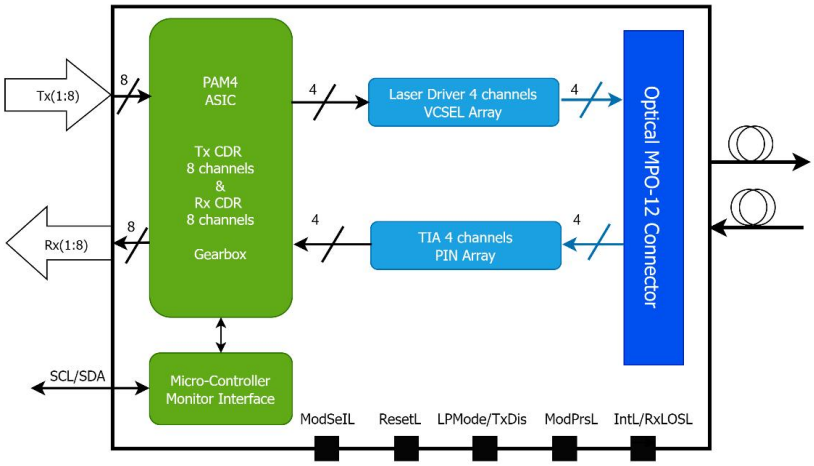

Figure 3 Transceiver Block Diagram

Optical Port Description

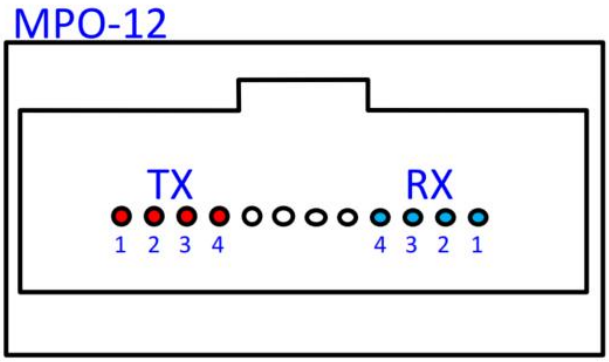

Figure4 Outside View of the QSFPDD MPO-12 Receptacle

Digital Diagnostic Specifications

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range

Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%		
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Mechanical Dimensions

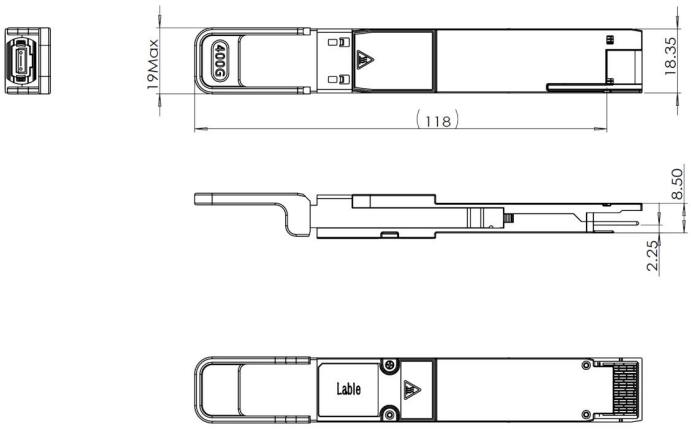

Figure 5. Mechanical Outline

Recommended Power Supply Filter

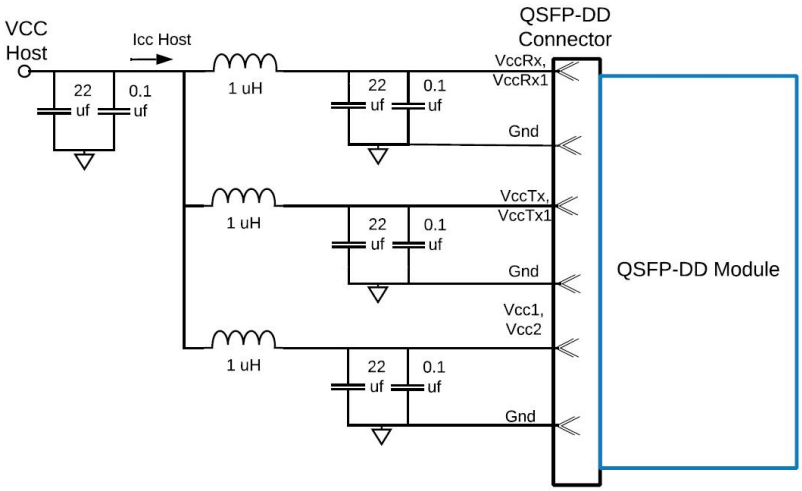

Figure 6. Recommended Power Supply Filter

ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class I Laser Product, or Class 1 Laser Product according to IEC/EN 60825-1:2014.

This product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.