

200Gb/s QSFP56 FR4 1310nm 2km Optical Transceiver

Features

- IEEE802.3bs 200GBASE-FR4 compliant
- QSFP56 MSA compliant
- 4 CWDM lanes MUX/DEMUX design
- Supports 212.5Gb/s aggregate bit rate
- Up to 2km transmission on single mode fiber (SMF) with FEC
- Operating case temp Commercial: 0°C to +70 °C
- 200GAUI-4 electrical interface
- Maximum power consumption 5W
- LC duplex connector
- RoHS compliant

Applications

- Data Center Interconnect
- 200G Ethernet
- Enterprise networking

Description

This product is a 200Gb/s transceiver module designed for 2km optical communication applications. The design is compliant to IEEE802.3bs 200GBASE-FR4 standard. The module converts 4 inputs channels (ch) of 50Gb/s (PAM4) electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 200Gb/s(PAM4) optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 200Gb/s(PAM4) input into 4 CWDM channels signals, and converts them to 4 channel output electrical data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. It contains a duplex LC connector for the optical interface and a 38-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module. Host FEC is required to support up to 2km fiber transmission.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP56 Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Functional Description

This product converts the 4-channel 200Gb/s(PAM4) electrical input data into CWDM optical signals (light), by a driven 4-wavelength EMLs. The light is combined by the MUX parts as a 200Gb/s data, propagating out of the transmitter module from the SMF. The receiver module accepts the 200Gb/s CWDM optical signals input, and de-multiplexes it into 4 individual 50Gb/s channels with different wavelength. Each wavelength light is collected by a discrete photo diode, and then outputted as electric data after amplified by a TIA and a post amplifier. Analog CDR is used to recovery PAM4 signals. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMODE, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2- wire serial communication commands. The ModSelL allows the use of this product on a single 2 - wire interface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP+ memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMODE) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state.

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Interrupt (IntL) is an output pin. “Low” indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

| Parameter | Symbols | Min. | Typical | Max. | Unit | Notes |
|-------------------------------------|---------|------|---------|------|------|-------|
| Storage Temperature | TS | -40 | | +85 | degC | |
| Operating Case Temperature | TOP | 0 | | 70 | degC | |
| Power Supply Voltage | VCC | -0.5 | | 3.6 | V | |
| Relative Humidity(non-condensation) | RH | 0 | | 85 | % | |
| Damage Threshold, each Lane | THd | 3.5 | | | dBm | |

Recommended Operating Conditions

Table2-Recommended Operating Conditions

| Parameter | Symbols | Min. | Typical | Max. | Unit | Notes |
|----------------------------|---------|-------|---------|----------------------|------|-------|
| Operating Case Temperature | Top | 0 | | +70 | degC | |
| Power Supply Voltage | VCC | 3.135 | 3.3 | 3.465 | V | |
| Data Rate, each Lane | | | 26.5625 | | GBd | |
| | | | 53.125 | | Gb/s | |
| Data Rate Accuracy | | -100 | | 100 | ppm | |
| Pre-FEC Bit Error Ratio | | | | 2.4x10 ⁻⁴ | | |
| Post-FEC Bit Error Ratio | | | | 1x10 ⁻¹² | | 1 |
| Control Input Voltage High | | 2 | | VCC | V | |
| Control Input Voltage Low | | 0 | | 0.8 | V | |
| Link Distance with G.652 | D | 0.002 | | 2 | km | 2 |

Notes:

[1]FEC provided by host system.

[2]FEC required on host system to support maximum distance.

Electrical Characteristic

Table3-Electrical Characteristic

| Parameter | Symbol | Min. | Typical | Max. | Unit | Notes |
|---|-----------------|----------------------------------|---------|------|------|-------|
| Supply current | I _{cc} | | | 1.52 | A | |
| Power Consumption | | | | 5 | W | |
| Optical Transmitter Characteristics | | | | | | |
| Signaling Rate, each Lane | TP1 | 26.5625 ± 100 ppm | | | GBd | |
| Differential pk-pk Input Voltage Tolerance | TP1a | 900 | | | mVpp | 1 |
| Differential Termination Mismatch | TP1 | | | 10 | % | |
| Differential Input Return Loss | TP1 | IEEE 802.3-2015 Equation (83E-5) | | | dB | |
| Differential to Common Mode Input Return Loss | TP1 | IEEE 802.3-2015 Equation (83E-6) | | | dB | |
| Module Stressed Input Test | TP1a | See IEEE 802.3bs 120E.3.4.1 | | | | 2 |
| Single-ended Voltage Tolerance Range (Min) | TP1a | -0.4 to 3.3 | | | | |
| DC Common Mode Input Voltage | TP1 | -350 | | 2850 | mV | 3 |
| Optical Receiver Characteristics | | | | | | |
| Signaling Rate, each lane | TP4 | 26.5625 ± 100 ppm | | | GBd | |
| Differential Peak-to-Peak | TP4 | | | 900 | mVpp | |
| Output Voltage | | | | | | |
| AC Common Mode Output Voltage, RMS | TP4 | | | 17.5 | mV | |
| Differential Termination Mismatch | TP4 | | | 10 | % | |
| Differential Output Return Loss | TP4 | IEEE 802.3-2015 Equation (83E-2) | | | | |
| Transition Time, 20% to 80% | TP4 | 9.5 | | | ps | |
| Near-end Eye Symmetry Mask Width (ESMW) | TP4 | | 0.265 | | UI | |
| Near-end Eye Height, | TP4 | 70 | | | mV | |

| | | | | | | |
|--|-----|------|-----|------|----|---|
| Differential | | | | | | |
| Far-end Eye Symmetry Mask Width (ESMW) | TP4 | | 0.2 | | UI | |
| Far-end Eye Height, Differential | TP4 | 30 | | | mV | |
| Far-end Pre-cursor ISI Ratio | TP4 | -4.5 | | 2.5 | % | |
| Common Mode Output Voltage (Vcm) | TP4 | -350 | | 2850 | mV | 3 |

Notes:

[1] With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.

[2] Meets BER specified in IEEE 802.3bs 120E.1.1.

[3] DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Optical Characteristics

Table4-Optical Characteristics

| Parameter | Symbols | Min. | Typical | Max. | Unit | Notes |
|---|------------------|------------------|---------|--------|------|---------------|
| Wavelength Assignment | L0 | 1264.5 | 1271 | 1277.5 | nm | |
| | L1 | 1284.5 | 1291 | 1297.5 | nm | |
| | L2 | 1304.5 | 1311 | 1317.5 | nm | |
| | L3 | 1324.5 | 1331 | 1337.5 | nm | |
| Transceiver | | | | | | |
| Data Rate, each Lane | | 26.5625 ±100 ppm | | | GBd | |
| Modulation Format | | PAM4 | | | | |
| Side-mode Suppression Ratio | SMSR | 30 | | | dB | Modulated |
| Total Average Launch Power | P _T | | | 10.7 | dBm | |
| Average Launch Power, each Lane | P _{AVG} | -4.2 | | 4.7 | dBm | 1 |
| Outer Optical Modulation Amplitude (OMA _{outer}), each Lane | P _{OMA} | -1.2 | | 4.5 | dBm | 2 |
| Launch Power in OMA _{outer} minus TDECQ, each Lane | | -2.6 | | | dB | For ER ≥4.5dB |
| | | -2.5 | | | dB | For ER ≤4.5dB |
| Transmitter and Dispersion Eye Closure for PAM4, each Lane | TDECQ | | | 3.3 | dB | |
| Extinction Ratio | ER | 3.5 | | | dB | |

| | | | | | | |
|--|------------------|------|------------------|------|-------|-------------------|
| Difference in Launch Power between any Two Lanes (OMA _{outer}) | | | | 4 | dB | |
| RIN _{16.5OMA} | RIN | | | -132 | dB/Hz | |
| Optical Return Loss Tolerance | TOL | | | 16.5 | dB | |
| Transmitter Reflectance | T _R | | | -26 | dB | |
| Average Launch Power of OFF Transmitter, each Lane | P _{off} | | | -20 | dBm | |
| Receiver | | | | | | |
| Data Rate, each Lane | | | 26.5625 ±100 ppm | | GBd | |
| Modulation Format | | | PAM4 | | | |
| Damage Threshold, each Lane | TH _d | 5.7 | | | dBm | 3 |
| Average Receive Power, each Lane | | -8.2 | | 4.7 | dBm | 4 |
| Receive Power (OMA _{outer}), each Lane | | | | 4.5 | dBm | |
| Difference in Receiver Power between any Two Lanes (OMA _{outer}) | | | | 4.1 | dB | |
| Receiver Sensitivity (OMA _{outer}), each Lane | SEN | | | -6.0 | dBm | For BER of 2.4E-4 |
| Stressed Receiver Sensitivity (OMA _{outer}), each Lane | SRS | | | -3.6 | dBm | 5 |
| Receiver Reflectance | R _R | | | -26 | dB | |
| LOS Assert | LOSA | -30 | | | dBm | |
| LOS De-assert | LOSD | | | -12 | dBm | |
| LOS Hysteresis | LOSH | 0.5 | | | dB | |
| Stressed Conditions for Stress Receiver Sensitivity (Note 6) | | | | | | |
| Stressed Eye Closure for PAM4 (SECQ), Lane under Test | | 0.9 | | 3.4 | dB | |
| OMA _{outer} of each Aggressor Lane | | | 1.5 | | dBm | |

Notes:

[1] Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

[2] Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 4.5 dB, the OMA_{outer} (min) must exceed the minimum value specified here.

[3] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.

[4]Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

[5]Measured with conformance test signal for BER = 2.4×10^{-4} .

[6]These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digital Diagnostic Functions

Table5-Digital Diagnostic Functions

| Parameter | Symbols | Min. | Max. | Unit | Notes |
|---|--------------|------|------|------|----------------------------------|
| Temperature monitor absolute error | DMI_Temp | -3 | 3 | degC | Over operating temperature range |
| Supply voltage monitor absolute error | DMI_VCC | -0.1 | 0.1 | V | Over full operating range |
| Supply voltage monitor absolute error | DMI_RX_Ch | -2 | 2 | dB | 1 |
| Channel Bias current monitor | DMI_Ibias_Ch | -10% | 10% | mA | |
| Channel TX power monitor absolute error | DMI_TX_Ch | -2 | 2 | dB | 1 |

Notes:

[1] Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Pin Description

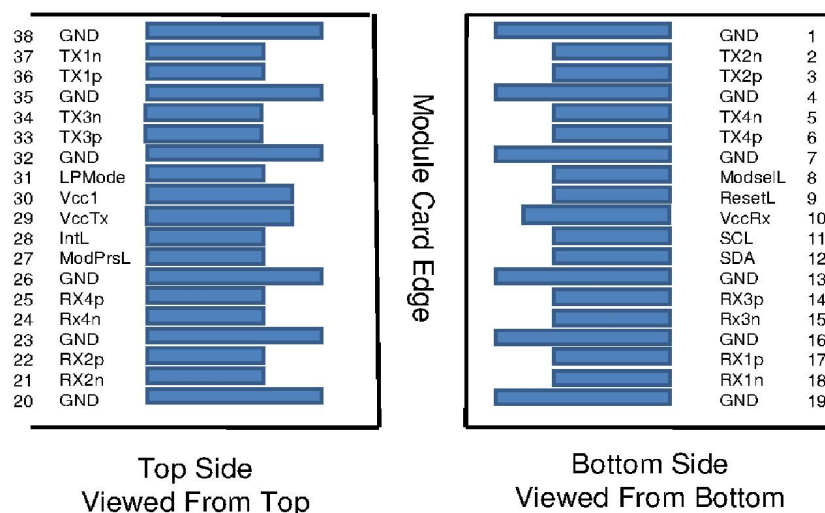


Figure 1 Pin view

Pin Function Definitions

Table6-Pin Function Definitions

| Pin | Symbols | Description | Notes |
|-----|---------|-------------------------------------|-------|
| 1 | GND | Ground | 1 |
| 2 | Tx2n | Transmitter Inverted Data Input | |
| 3 | Tx2p | Transmitter Non-Inverted Data Input | |
| 4 | GND | Ground | 1 |
| 5 | Tx4n | Transmitter Inverted Data Input | |
| 6 | Tx4p | Transmitter Non-Inverted Data Input | |
| 7 | GND | Ground | |
| 8 | ModSelL | Module Select | |
| 9 | ResetL | Module Reset | |
| 10 | Vcc Rx | +3.3V Power Supply Receiver | 2 |
| 11 | SCL | 2-wire serial interface clock | |
| 12 | SDA | 2-wire serial interface data | |
| 13 | GND | Ground | |
| 14 | Rx3p | Receiver Non-Inverted Data Output | |
| 15 | Rx3n | Receiver Inverted Data Output | |
| 16 | GND | Ground | 1 |
| 17 | Rx1p | Receiver Non-Inverted Data Output | |
| 18 | Rx1n | Receiver Inverted Data Output | 1 |
| 19 | GND | Ground | 1 |
| 20 | GND | Ground | |

| | | | |
|----|---------|-------------------------------------|---|
| 21 | Rx2n | Receiver Inverted Data Output | |
| 22 | Rx2p | Receiver Non-Inverted Data Output | |
| 23 | GND | Ground | |
| 24 | Rx4n | Receiver Inverted Data Output | |
| 25 | Rx4p | Receiver Non-Inverted Data Output | |
| 26 | GND | Ground | 1 |
| 27 | ModPrsL | Module Present | |
| 28 | IntL | Interrupt | |
| 29 | VccTx | +3.3V Power supply transmitter | 2 |
| 30 | Vcc1 | +3.3V Power supply | 2 |
| 31 | LPMode | Low Power Mode | |
| 32 | GND | Ground | 1 |
| 33 | Tx3p | Transmitter Non-Inverted Data Input | |
| 34 | Tx3n | Transmitter Inverted Data Input | |
| 35 | GND | Ground | 1 |
| 36 | Tx1p | Transmitter Non-Inverted Data Input | |
| 37 | Tx1n | Transmitter Inverted Data Input | |
| 38 | GND | Ground | 1 |

Notes:

[1]GND is the symbol for signal and supply (power) common for QSFP56 modules. All are common within the QSFP56 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

[2]VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure3 below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP56 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

Transceiver Block Diagram

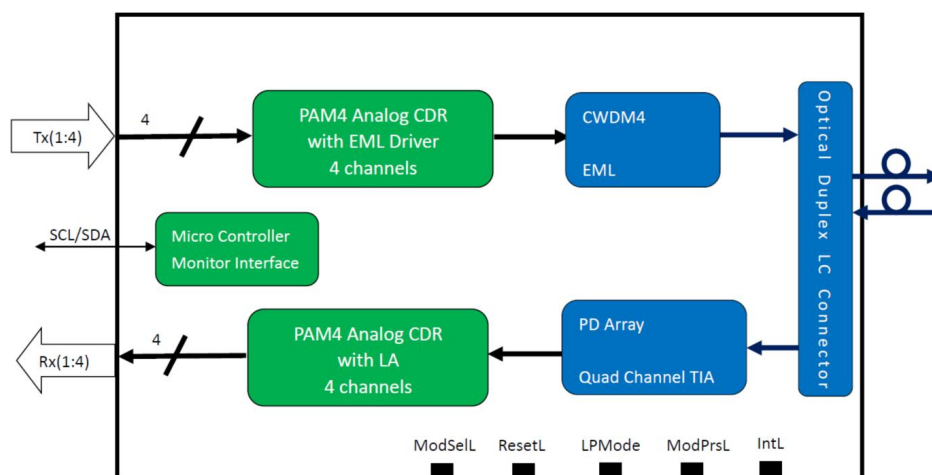


Figure 2 Transceiver Block Diagram

Mechanical Dimensions

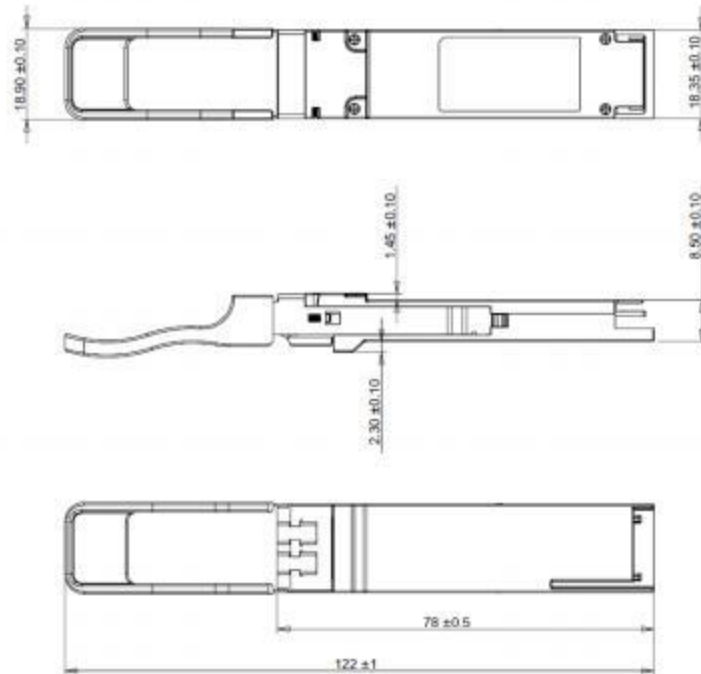


Figure 3 Mechanical Outline

ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 / JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.