

400Gb/s QSFP-DD to QSFP-DD Active Optical Cable

Features

- Up to 53.125Gbps Data Rate per Channel by PAM4 Modulation
- Support 400GAUI-8 Electrical Interface
- Integrated 850nm VCSEL Array and PD Array
- DDM Function Implemented
- Hot-pluggable QSFP-DD Form Factor
- Maximum Link Length of 100m OM4 (MMF) Fiber
- Low Power Dissipation: $\leq 11W$
- Single +3.3V Power Supply
- Operating Temperature Range: 0°C~+70 °C
- Compliant with RoHS10

Applications

- Data Centers and Cloud Networks
- Other 400G Interconnect Requirement

Description

400G QSFP-DD to 400G QSFP-DD Active Optical Cable enables low-power, high-reliability and high-speed interconnections over very thin copper cables without using any optical components. It is designed for relatively short connection, offering high-density solution alternative for system providers and customers implementing 400G in data centers and Cloud Networks. It is compliant with IEEE 802.3cd, OIF-CEI-04.0, QSFP-DD MSA and QSFP-DD-CMIS-rev4p0.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Storage Temperature Range	TS	-20	-	+85	°C	
Relative Humidity	RH	0	-	85	%	
Power Supply Voltage	VCC	-0.5	-	+4.0	V	

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbol	Unit.	Min	Typ.	Max	Note
Operating Case Temperature Range	Tca	°C	0		70	
Power Supply Voltage	VCC	V	3.135	3.3	3.465	
Bit Rate [per Channel]	BR	GBd		26.5625		
Humidity	Rh	%	5		85	
Fiber Bend Radius	Rb	cm	3			

Electric Specifications

Table3-Electrical Characteristics

Parameter	Symbol	Unit	Min.	Typical	Max.	Note
Supply Voltage	VCC VCC3.3-Tx VCC3.3-Rx	V	3.135	3.3	3.465	
Power Consumption	Pc	W		9.5		Per-end
Transceiver Power-on Initialize Time		ms			2000	
Transmitter						
Differential Peak-to-peak input Voltage Tolerance		mV	900			
Differential Termination Mismatch					10%	
Differential Input Return Loss(SDD11)		dB			See CEI-56G-	

					VSR	
Common-mode to Differential Conversion and Differential to Common-mode Conversion(SCD11, SDC11)		dB			See CEI-56G- VSR	
Receiver						
Differential Peak-to-peak Output Voltage		mV			900	
DC Common Mode Voltage	V _{cm}	mV	-350		2850	
AC Common Mode Noise, RMS		mV			17.5	
Differential Termination Mismatch		%			10	
Differential Output Return Loss(SDD22)		dB			See CEI-56G- VSR	
Common-mode to Differential Conversion and Differential to Common-mode Conversion(SCD22, SDC22)		dB			See CEI-56G- VSR	
IIC communication						
IIC Clock Frequency (QSFP-DD)		KHZ		400	1000	
Clock Stretching		us			500	
Data Hold Time		ns				

Principle Diagram

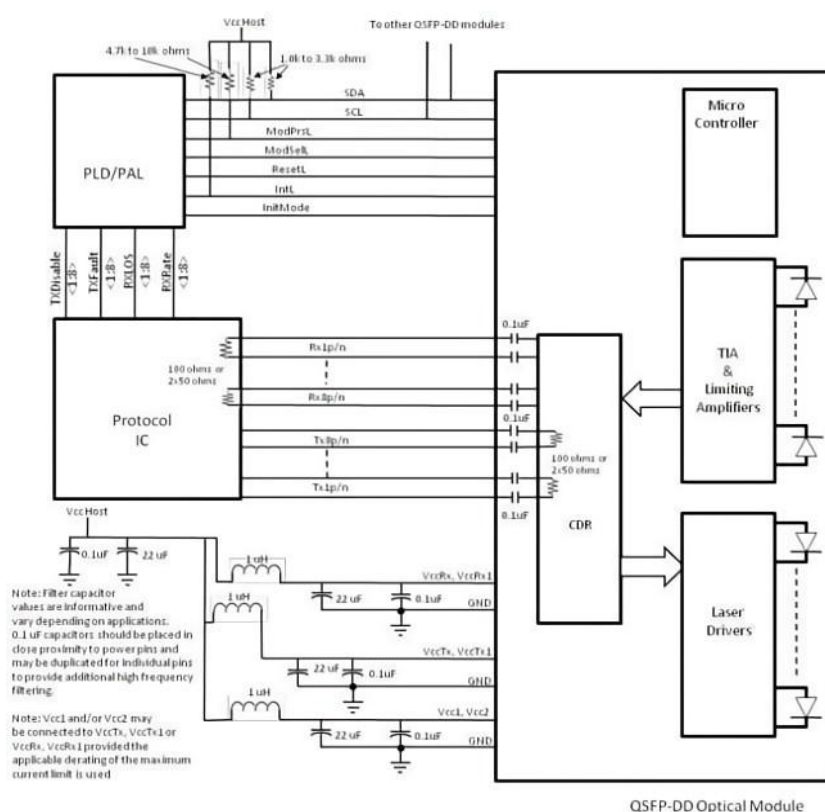


Figure 1 Module Principle Diagram

Pin Descriptions

Table4-Pin Description				
Pin	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	1
18	CML-O	Rx1n	Receiver Inverted Data Output	1
19		GND	Ground	
20		GND	Ground	
21	CML-O	Rx2n	Receiver Inverted Data Output	1
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	
27	LVTTL-O	ModPrsL	Module Present	2
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636)	2
29		VccTx	+3.3V Power supply transmitter	
30		Vcc1	+3.3V Power supply	1
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	
32		GND	Ground	
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	1
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	1

37	CML-I	Tx1n	Transmitter Inverted Data Input	1
38		GND	Ground	
39		GND	Ground	
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		VccRx1	3.3V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future Use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69		Reserved	For future Use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All the common within the QSFP-DD module and all

module voltages are referenced to this potential unless otherwise noted. Connected these directly to the host board signal common ground plane.

2. VCCR_x, VCCR_x 1, VCC1, VCC2, VCCT_x, and VCCT_x 1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4 . VCCR_x, VCCR_x 1, VCC 1, VCC2, VCCT_x, and VCCT_x 1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor Specific and Reserved pads shall have an impedance to GND that is greater than 10kOhms and less than 100pF.

Mechanical Dimensions

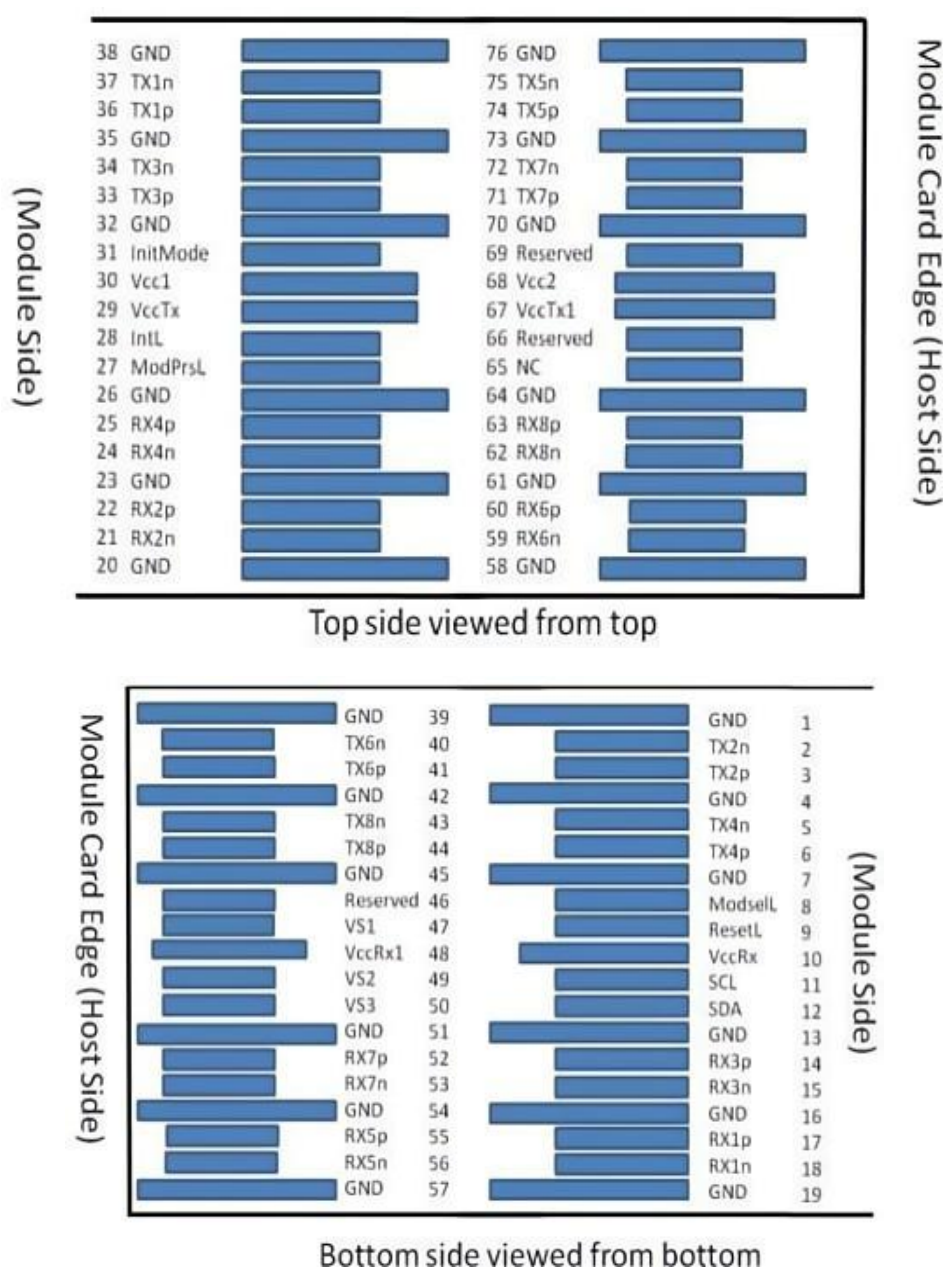


Figure 2. Electrical Pin-out Details

Module Memory Map

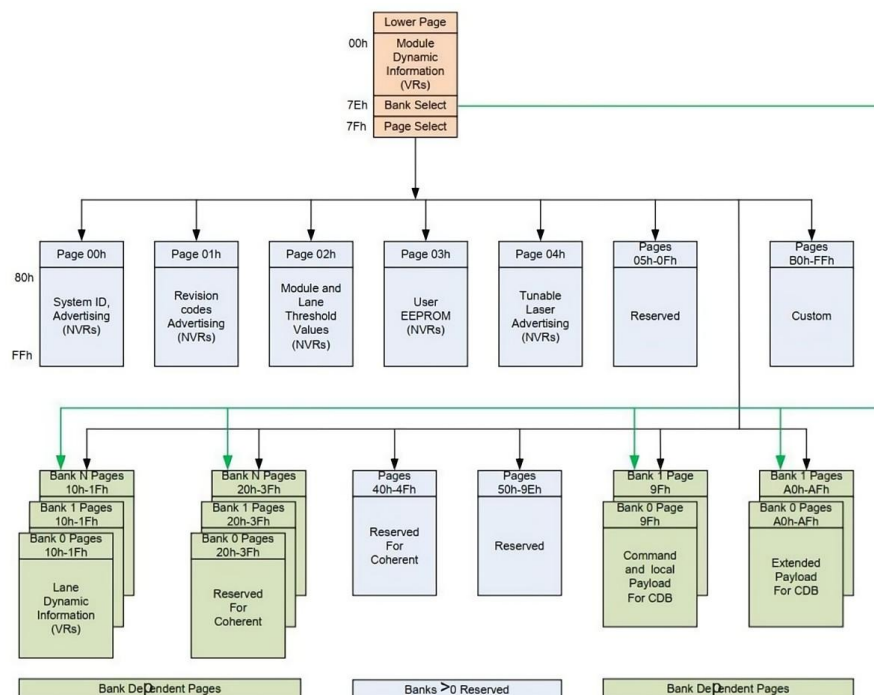


Figure 3. Digital Diagnostic Memory Maps

Host Board Power Supply Filtering

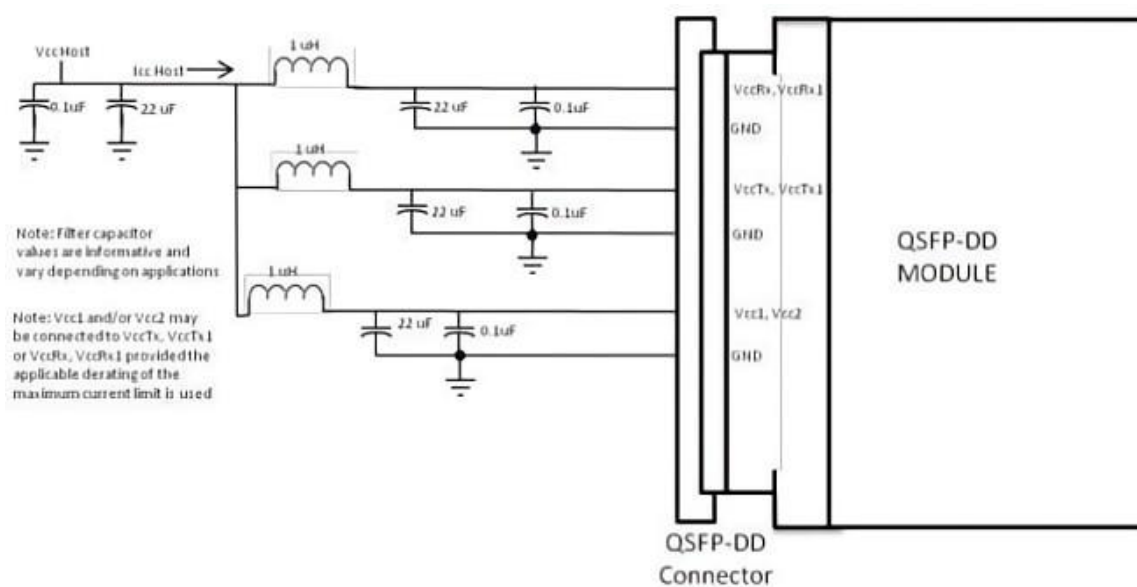


Figure 4. Digital Diagnostic Memory Map

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Edge Card Connector. Figure is the suggested transceiver/host interface.

Mechanical

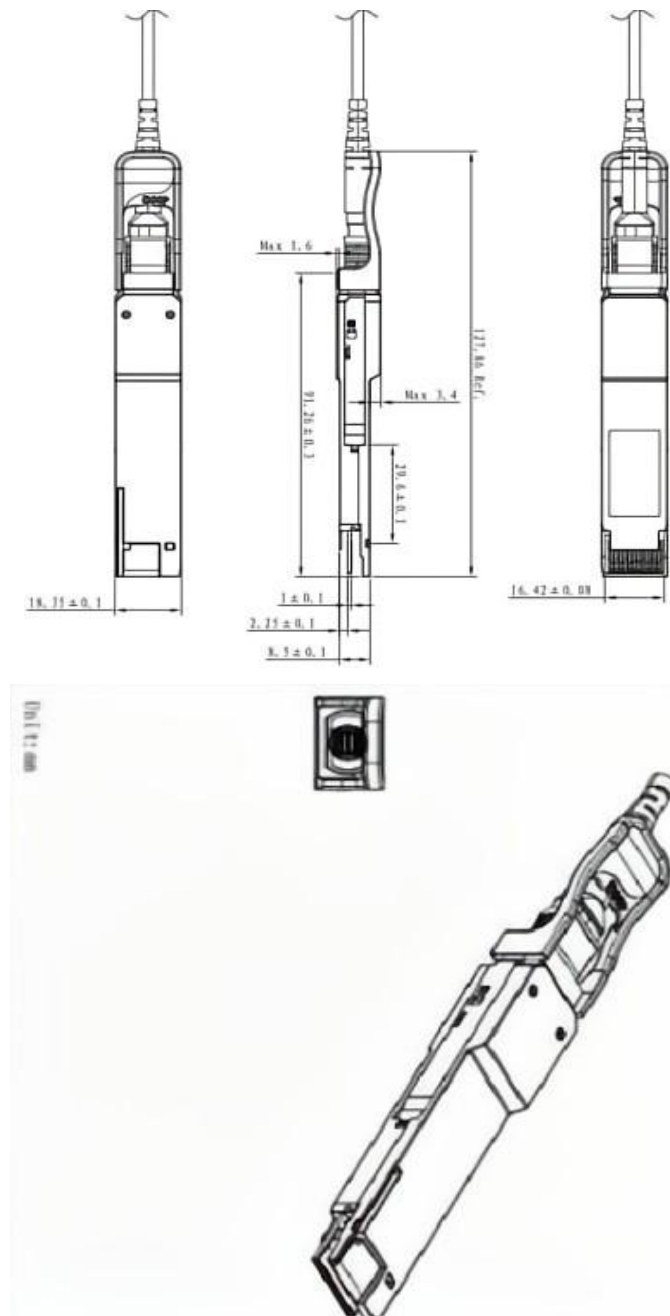


Figure 5. Package Outline